Development of a Multi-Purpose Logic Module with the FPGA

K. Nanbu , T. Ishikawa , and H. Shimizu

Laboratory of Nuclear Science, Tohoku University, Sendai, 982-0826

We have developed a multi-purpose logic module (MPLM) with an FPGA. The internal circuit of this module can be modified easily with the FPGA. This kind of module enables trigger pulse processing for nuclear science. As a first step, the MPLM is used as an event tag generator in experiments with the FOREST detector system.

§1. Introduction

The structure and production mechanism of hadrons have been experimentally investigated via meson photo-production in Laboratory of Nuclear Science, Tohoku University. Nucleon resonances will be studied intensively with an electro-magnetic calorimeter complex FOREST in the GeV-γ experimental hall. Since the number of detectors in the FOREST is about 800, a set of logic modules for specified purposes is expensive. Therefore, a multi-purpose logic module with a field programmable gate array (FPGA) has been developed.

§2. Feature of FPGA

An FPGA is a semiconductor device which is programmable for any logic function by a designer. The FPGA is usually slower than an application-specific integrated circuit (ASIC). Since the ASIC cannot be modified after the design is completed, it is difficult to handle an ASIC to implement a specified design without bugs. On the other hand, the FPGA can be reconfigurable like software on a personal computer after it is manufactured. It is easy to shorten designing time to obtain the specified logic function by a trial-and-error method.

The FPGA contains programmable logic components called logic blocks, and programmable interconnects. Logic blocks can be programmed to operate simple or combinatorial functions of basic logic gates (AND, OR, XOR, flip-flops, and so on). The FPGA manufactured by Xilinx contains configurable logic blocks (CLB), input/output blocks (IOB), block random access memories (RAM), multipliers, and digital clock managers (DCM). The internal circuit of FPGA is constructed by connecting these elements.

The behavior of FPGA is usually defined with a hardware description language (HDL). Configuration data of logic blocks and interconnects which are fitted to the actual FPGA architecture are generated by a FPGA design software. The data are typically downloaded via a Joint Test Action Group (JTAG)

link cable.

§3. Multi-Purpose Logic Module

We have developed a logic module called Multi-Purpose Logic Module (MPLM) with an FPGA. This module is packaged in a single-width nuclear Instrumentation module (NIM) module. Figure 1 shows a photo of the MPLM. The FPGA used is a Xilinx SPARTAN3, and contains 4320 flip-flops (FF), 256 Kbit RAM, and 200,000 system gates.

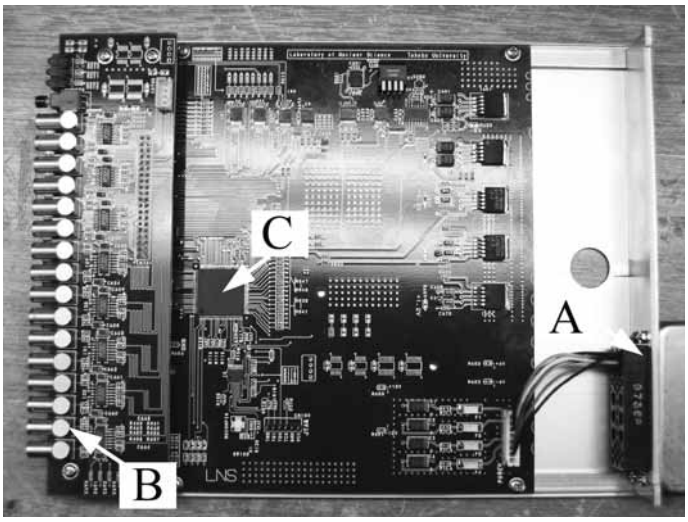

Fig.1. The MPLM (A: Bin power, B: LEMO Connector, C: FPGA).

This newly developed module accepts NIM standard signals, through 16 input and output channels. Since the FPGA does not accept the NIM signal, additional level converters between the NIM standard and the Low Voltage Transistor-Transistor Logic Level (LVTTL) signals are employed. The propagation delay from the input to the output is less than 10 ns, in which the conversion time from the NIM to LVTTL signals is dominant.

Figure 2 shows the block diagram of the MPLM. The MPLM contains 16 inputs with NIM to LVTTL converters, 16 outputs with LVTTL to NIM converters, a peripheral circuit for the configuration of the FPGA, a clock signal, and 3 status light emitting diodes (LED). The clock signal is generated by a crystal oscillator with a frequency of 33.33 MHz, and the frequency stability is better than 100 ppm. The FPGA receives a clock signal through a built–in global buffer (GBUF). The power source for many devices in the MPLM is provided through regulated power supplies as shown in Fig. 2. The MPLM supports the In-System Programming (ISP) through the JTAG interface, and a FPGA configuration system in a Platform Flash Memory (PROM). This module detects failures of the clock signal and those of power system. An RS-232C interface to a personal computer is optionally available. An operational amplifier (OPAMP) is operated with a higher frequency to shorten the leading time of the NIM standard signal ($\sim$3 nsec). The input impedance of the OPAMP is rather low for the FPGA. Nevertheless, the generated signal with the

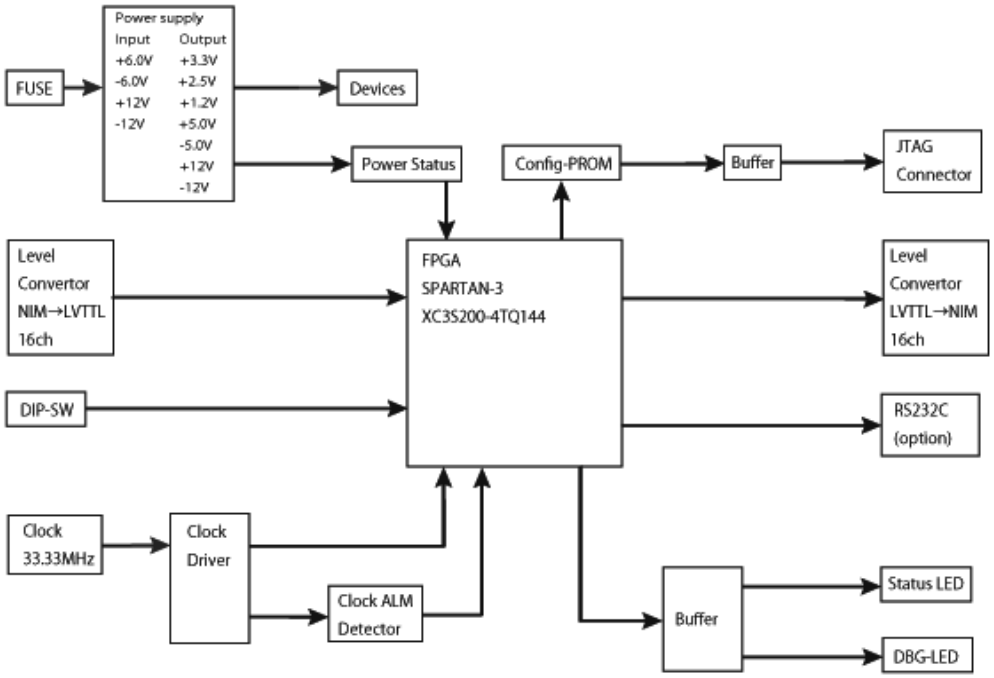

Fig.2. Block diagram of the MPLM.

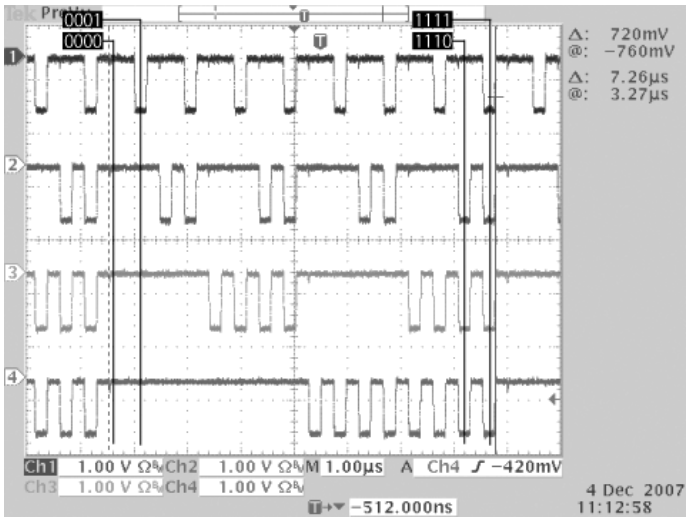

Fig.3. Timing diagram of the 4bit binary counter implemented in the MPLM. The 1st and 4th channels correspond to the lowest and most significant bits, respectively.

OPAMP meets the NIM standard although some reflection is observed in a pulse of the signal due to the impedance mismatch. Since this module is constructed on a 4 layer printed-circuit board (PCB), the impedance of the power system is reduced, which results in the noise level suppressed, in addition the high frequency operation allows the use of surface-mount components.

As a first step, this module is used as an event tag generator in experiments. A data taking system for FOREST is divided into several subsystems to collect digitized data with a short dead time. The

event tag is important to check event consistency whether digitized data collected by these subsystems belong to the same event or not. When the generator receives a trigger accept signal, a 4 bit associated event tag is generated. Figure 3 shows the operation of a 4 bit binary counter in the MPLM.

§4. Conclusion

A Multi-purpose Logic Module has been developed. This kind of module is necessary to handle digitized data efficiently under complicated trigger conditions.